AIP Applied Physics Letters

Vertically integrated double-layer on-chip silicon membranes for 1-to-12 waveguide fanouts

Yang Zhang, Amir Hosseini, Jaehyun Ahn, David N. Kwong, Babak Fallahazad et al.

Citation: Appl. Phys. Lett. **100**, 181102 (2012); doi: 10.1063/1.4709489
View online: http://dx.doi.org/10.1063/1.4709489
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v100/i18
Published by the American Institute of Physics.

Related Articles

High-speed waveguide-coupled graphene-on-graphene optical modulators
Appl. Phys. Lett. 100, 171107 (2012)

High-efficiency acousto-optical interaction in phoxonic nanobeam waveguide
Appl. Phys. Lett. 100, 171103 (2012)

Perpendicular coupling to in-plane photonics using arc waveguides fabricated via two-photon polymerization
Appl. Phys. Lett. 100, 171102 (2012)

Grating-coupled silicon microring resonators
Appl. Phys. Lett. 100, 121118 (2012)

Waveguide-integrated near-infrared detector with self-assembled metal silicide nanoparticles embedded in a silicon p-n junction
Appl. Phys. Lett. 100, 061109 (2012)

Additional information on Appl. Phys. Lett.

Journal Homepage: http://apl.aip.org/
Journal Information: http://apl.aip.org/about/about_the_journal
Top downloads: http://apl.aip.org/features/most_downloaded
Information for Authors: http://apl.aip.org/authors

ADVERTISEMENT

ACCELERATE AMBER AND NAMD BY 5X.
TRY IT ON A FREE, REMOTELY-HOSTED CLUSTER.
LEARN MORE

Downloaded 30 Apr 2012 to 129.116.140.200. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

Vertically integrated double-layer on-chip silicon membranes for 1-to-12 waveguide fanouts

Yang Zhang,[a] Amir Hosseini, Jaehyun Ahn, David N. Kwong, Babak Fallahazad, Emanuel Tutuc, and Ray T. Chen[b]
Microelectronic Research Center, Department of Electrical and Computer Engineering, The University of Texas, 10100 Burnet Rd. Austin, Texas 78758, USA

(Received 13 February 2012; accepted 14 April 2012; published online 30 April 2012)

We present an on-chip vertically integrated three-dimensional photonic integrated circuit. Double-layer 1×12 multimode interference (MMI) couplers are fabricated on silicon membranes using double-bonded silicon-on-insulator wafers. The input light is transverse electric polarized, operating at 1550 nm. The top layer MMI coupler has an excess loss of 0.48 dB and an uniformity within 1.1 dB. The bottom layer MMI coupler has an excess loss of 2.9 dB and an uniformity within 1.7 dB. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4709489]

Large on- and off-chip bandwidths required for high performance multi-core structures (∼10TB/s by 2015) corresponding to interconnect energy budgets of ∼100 fJ/bit will render optical components essential parts of future high performance integrated systems.[1–3] Complementary metal-oxide-semiconductor (CMOS) compatible silicon photonics, which allows for integration of optical components on the same silicon chip with CMOS transistors, is considered one of the solutions to such a high demand for low energy and high bandwidth communications.[3,4] Since the Luxtera silicon photonic chip in 2002, the number of on-chip photonic components has doubled each year.[5,6] There is also a "Moore's law like" trend observed in InP-based photonic integrated circuit (PIC) development since 1988.[7] However, due to the large sizes of the on-chip photonic components, single layer photonic component counts cannot exceed 1000 and 10 000 in InP and silicon PICs, respectively.[8]

Vertical integration of multiple layers of active and passive components can resolve the problem of limited real estate on a single layer.[9] So far, an extra polysilicon layer on top of the crystalline silicon layer has been used for CMOS microelectronics and photonics integration.[10,11] This scheme may also be used for three-dimensional (3D) photonics integration. However, the optical losses in polysilicon waveguides are dominated by scattering and absorption at the grain boundaries,[10] which increase significantly when the waveguide width shrinks to below 200 nm.[12] Techniques such as high temperature annealing, special hydrogen plasma passivation steps, and patterning waveguides before the solid-phase crystallization (SPC) of deposited amorphous silicon were shown to reduce the propagation loss.[12,13] Lowest losses ranging from 7 dB/cm to 13 dB/cm were reported in polycrystalline silicon waveguides with cross sectional dimensions of approximately 450 nm × 250 nm[12,14,15] and from 1 dB/cm to 2 dB/cm in crystalline silicon waveguides with similar dimensions.[16,17] Additionally, if the temperature process is limited to about 600 °C, which is compatible with standard CMOS processes, the Q-factor of the ring resonators fabricated on polysilicon layers drops by an order of magnitude,[10,18] indicating even higher losses.

In this paper we demonstrate a 3D photonic integration of self-aligned structures using double-bonded silicon-on-insulator (SOI) wafers by fabricating double-layer 1×12 multimode interference (MMI) couplers on silicon membranes. Using the presented scheme, multi-levels of PICs including waveguide arrays, MxN MMI couplers, and arrayed waveguide gratings (AWGs) can be vertically integrated to significantly increase the on-chip integrated photonic component count.

The schematic of a $1 \times N$ MMI coupler is shown in Figure 1(a). We choose the MMI width, $W_{MMI} = 60\,\mu$m. The MMI length with a $1 \times N$ fanout is given as $L_{MMI} = (n_{eff} W_{MMI}^2)/(\lambda_0 N) = 664\,\mu$m,[19] where $n_{eff} = 3.43$ (for $1.3\,\mu$m thick silicon membrane) is the effective refractive index of the transverse electric (TE) fundamental mode of the multimode waveguide, and $\lambda_0 = 1.55\,\mu$m is the free space wavelength. The input and output access waveguide widths, $W_w = 2.5\,\mu$m, match the mode sizes of the input/output lensed fibers. Thus, the fiber-waveguide coupling tolerance is enhanced due to the waveguides' relatively large end-fire cross sections. The schematic of the double-bonded SOI wafer and self-aligned waveguide structure are shown in Figure 1(b). The thicknesses of both silicon layers are $h_1 = h_2 = 1.3\,\mu$m, and the two buried oxide (BOX) layers are both $2.0\,\mu$m thick. The simulated effective index of the fundamental TE and transverse magnetic (TM) modes in the access waveguides are 3.417 and 3.412, respectively, at $\lambda = 1.55\,\mu$m. Polarization independent operation is expected due to the small difference between the TE and TM effective indices. We fabricate two self-aligned 1×12 MMI couplers on two vertically stacked silicon membrane layers using one lithography process followed by a single etching step. MMI couplers can be used for efficient on-chip beam splitting.[19] A complete analysis for a symmetrically excited $1 \times N$ MMI coupler with uniform output was presented in Ref. 20.

The double-bonded SOI wafers are fabricated using fusion bonding and etch-back,[21] and are commercially available from Ultrasil. A 100 nm thick chromium etching mask is defined through an e-beam lithography and lift-off process. The pattern is then transferred to both silicon layers using

[a]Electronic mail: yangzhang@utexas.edu.
[b]Electronic mail: raychen@uts.cc.utexas.edu.

 © 2012 American Institute of Physics

Downloaded 30 Apr 2012 to 129.116.140.200. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

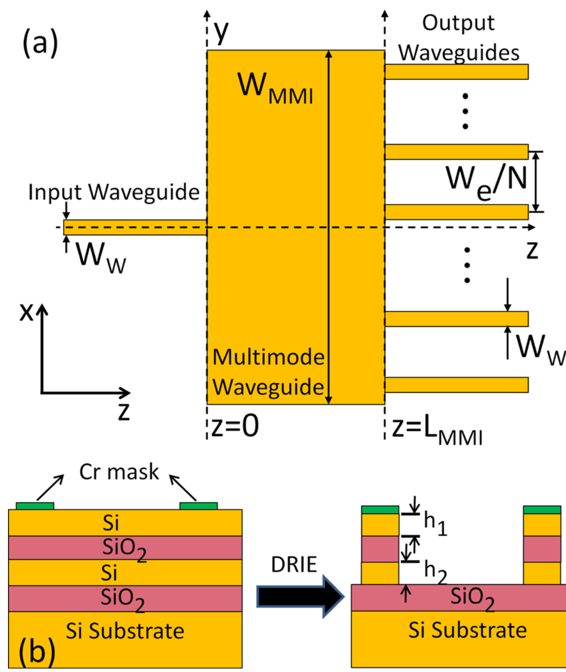

FIG. 1. (a) The Schematic of a 1 × N MMI coupler. (b) The schematic of the double-bonded SOI wafer and self-aligned waveguide structure.

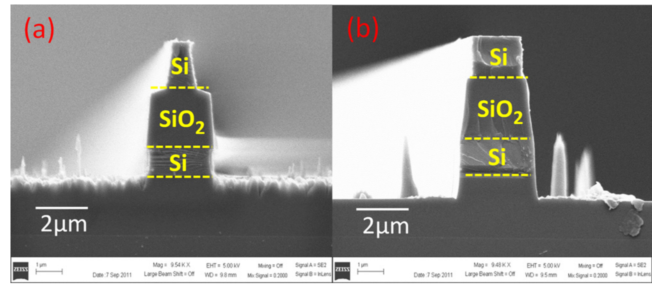

FIG. 2. SEM images of the waveguide cross section under different etching conditions. (a) A waveguide cross section with large undercut. (b) A waveguide cross section with corrected undercut.

one SF_6/C_4F_8/Ar based deep reactive-ion-etching (DRIE) step in Plasma-Therm's Versaline system. The DRIE process consists of ~1000 iterations of a two-step polymer deposition/etching cycle. Afterwards, the chromium mask is removed. The sidewall profile control in the DRIE process is the key to the performance of the fabricated devices. Although the Bosch process based DRIE of silicon, which alternates repeatedly between deposition of a polymer passive layer and isotropic plasma etching of silicon, is well developed in industry[22] and the standard recipes are provided by the system manufacturer, it has a very slow etch rate for silicon oxide and is not applicable for etching into double-bonded SOI wafers. In order to achieve a vertical sidewall, several process parameters need to be optimized, including gas composition, bias radio frequency (RF) voltage, inductively coupled plasma (ICP) power, chamber pressure, and step time. A standard recipe (Table I) for etching SOI wafers is used as the base recipe for parameter optimization. Wafer loading and temperature are kept constant during the optimization process.

By individually optimizing these parameters to achieve vertical sidewalls, we arrive at the final recipe, which is also shown in Table I. We determine that the bias RF voltage has the largest impact on the anisotropy of the sidewall profile. A larger bias RF voltage results in a higher etch rate and yields a more vertical sidewall profile during silicon oxide etching, but it also causes more damage to the polymer layer on the sidewall of the silicon membrane layer. Figure 2(a) shows the cross section of a waveguide etched using our otherwise final recipe with a 450 V bias RF voltage. The polymer layer on the sidewall is consumed during the etching step and results in a large undercut to the top silicon layer, leading to significant deviation from the original design. Figure 2(b) shows the cross section of a waveguide etched using the final recipe. The result shows a reduced undercut and a ~80° tapered sidewall profile during the silicon oxide etching. The undercut to the top silicon layer is inevitable due to the required ~40 min etch time of the BOX layer.[23]

The fabricated MMI access waveguides are 2.0 μm and 2.9 μm wide on the top and bottom layers, respectively. These access guides also correspond to TE fundamental mode effective refractive indices of 3.410 and 3.419, respectively [Figure 2(b)]. We note that because of the large thicknesses of the silicon layers, the effective index changes negligibly with variations in the waveguide width. Figure 3(a) shows a microscope image of the overall double-layer MMI. Figures 3(b) and 3(c) show the scanning electron microscope (SEM) images of the MMI output region and the output facet, respectively, with their corresponding locations labeled in Figure 3(a).

A six-axis automated aligner system with a movement precision of 50 nm is utilized to couple TE polarized light at a wavelength of 1550 nm from a polarization maintaining lensed fiber (PMF) with a 2.5 μm output mode diameter into the silicon waveguide inputs. An infrared (IR) camera connected to a variable objective lens captures the top-down, near-field images of the output facets. In order to visually resolve the 12 output spots, a waveguide fanout design is used to increase the separation of each adjacent channel to 30 μm [Figure 3(c)]. In order to visualize individual layer coupling in our double-layer device, we separate the outputs in the bottom layer from those in the top layer so that the

TABLE I. DRIE base and final parameters for one deposition and etching cycle.

	Gas flow rate (sccm[a])						Bias RF voltage (V)		ICP power (W)		Pressure (mTorr)		Time (s)	
	SF_6		C_4F_8		Ar									
Steps	Base	Final	Base	Final	Base	Final	Base	Final	Base	Final	Base	Final	Base	Final
Deposition	50	50	125	125	10	10	10	10	1600	1600	20	20	0.8	0.8
Etching	60	50	40	40	10	10	250	400	1200	1500	20	20	2	2

[a]SCCM denoted standard cubic centimeter per minute at standard temperature and pressure (STP).

Downloaded 30 Apr 2012 to 129.116.140.200. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

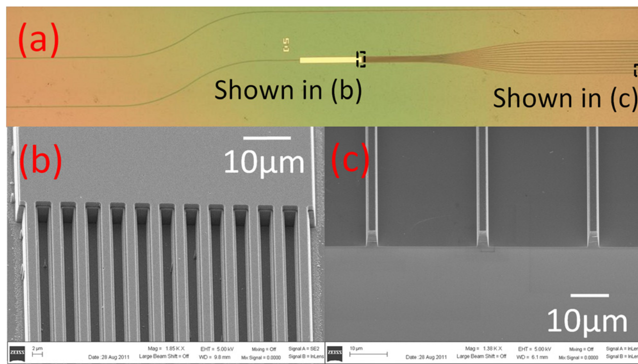

FIG. 3. (a) Optical microscope image of the double-layer MMI, (b) SEM image of the MMI output region, (c) SEM image of the output waveguide's facet.

two device layers terminate at two different locations as shown in Figure 4(a). Figures 4(b) and 4(c) illustrate the excitation of top and bottom layer MMI couplers, respectively. These results demonstrate selective coupling to each layer with negligible crosstalk, which in turn is due to the 2 μm thick BOX layer between the two silicon layers. Figure 4(d) illustrates the simultaneous excitation of top and bottom layer MMI couplers.

We characterize the MMI couplers on both layers by fiber scanning as described in Ref. 19. The chip is cleaved to make measurable facets via fiber for both the top and bottom layers. A single-mode lensed fiber (SMF) is used to scan each output channel to determine the output intensity of each channel and evaluate the performance of the MMI couplers on both layers. The uniformity of an MMI coupler is defined as $10\log(I_{max}/I_{min})$, where I_{max} and I_{min} are the maximum and minimum intensities of the MMI output channels. The excess loss of an MMI coupler, which excludes the fiber-to-waveguide coupling loss and the waveguide propagation loss, is defined as $-\log[(\sum I_m)/I_{in}]$, where I_m is the intensity of the mth output channel and I_{in} is the output intensity of a reference waveguide on the same chip with the same cross section dimensions as the MMI access waveguides. Using FIMMPROP's fully vectorial eigenmode decomposition-based complex film mode matching (FMM) solver (with 60 one-dimensional (1D) modes), we calculate the variations of the MMI excess loss and uniformity for both TE and TM polarizations [Figure 5]. Polarization independent operation is expected for a bandwidth larger than 30 nm.

The top layer MMI coupler has an excess loss of 0.48 dB and an uniformity within 1.1 dB, while the bottom layer MMI coupler has an excess loss of 2.9 dB and an uniformity within 1.7 dB. Since the input waveguide is multimode, the excitation of TE_{0n} and TE_{mn} (m and n are the horizontal and vertical orders of the mode, m, $n > 0$) modes depends on the input field launching condition and consequently contributes to the excess loss and output non-uniformity. In our case, the input lensed fiber mode size ($1/e^2$) is 2.5 μm $\times$ 2.5 μm, and the input waveguide TE_{00} mode size is 2.2 μm $\times$ 1.1 μm (1.6 μm $\times$ 1.1 μm) for the bottom (top) layer. With optimized input coupling conditions, input power is mostly coupled to the TE_{00} mode. The MMI

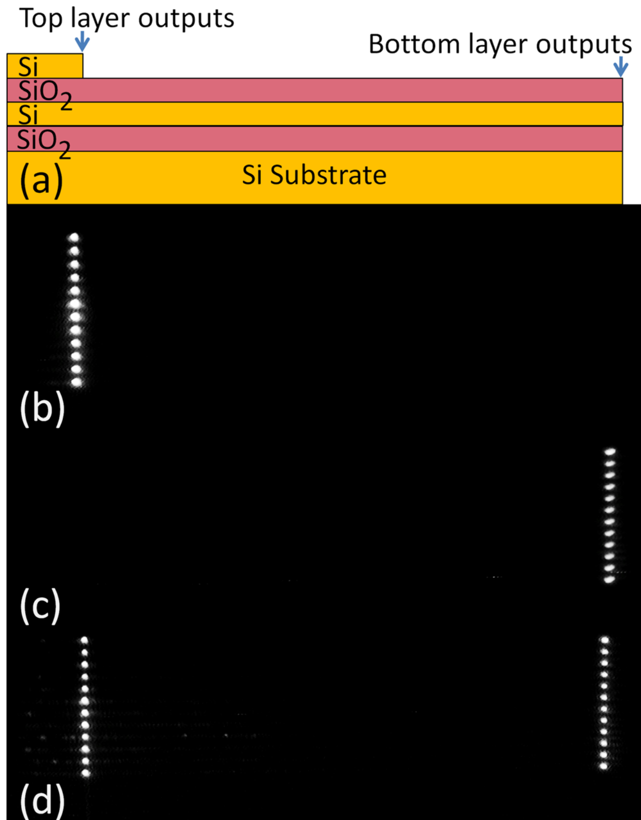

FIG. 4. (a) Schematic of separated outputs for the top and bottom layers. (b) IR top-down image of the double-layer MMI coupler with top layer excitation. (c) IR top-down image of the double-layer MMI coupler with bottom layer excitation. (d) IR top-down image of the double-layer MMI coupler with simultaneous excitation to both layers.

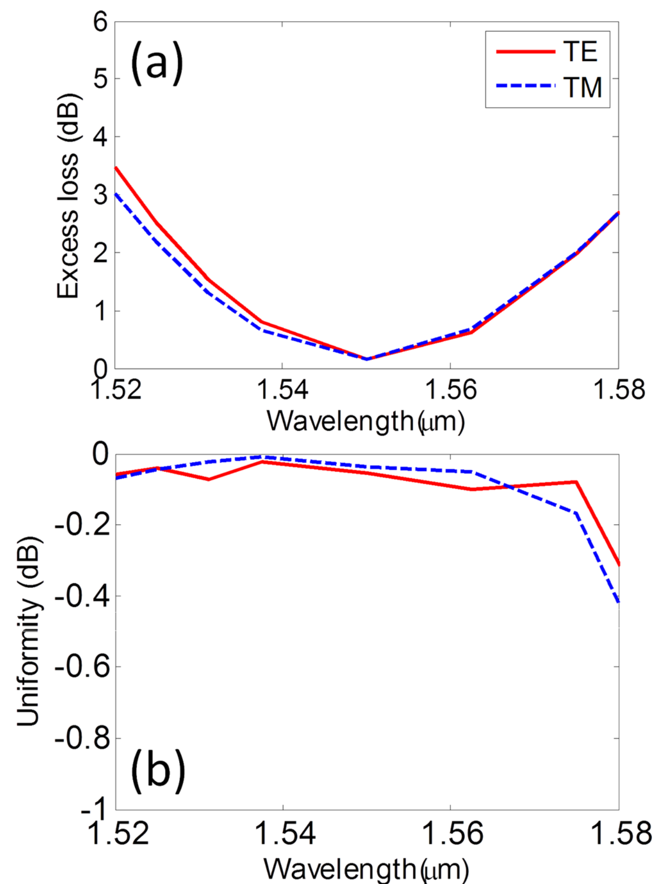

FIG. 5. Simulated MMI (a) excess loss and (b) uniformity as functions of wavelength for TE and TM polarizations.

Downloaded 30 Apr 2012 to 129.116.140.200. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

performance is most efficient for the TE_{00} mode due to having the highest effective modal index.[19] Under the excitation of the TE_{00} mode of the input waveguide, TE_{m0} modes will be excited, but TE_{0n} modes will not be excited inside the multimode waveguide region [Figure 1(a)]. By comparing the measured MMI performance metrics of both layers to $1 \times N$ MMIs fabricated on a 230 nm thick silicon nanomembrane (vertically single mode),[19] we confirm that the higher-order modes (inside the access waveguides) are suppressed with the optimized input coupling condition where most energy is coupled to the TE_{00} mode. We also find that bottom layer silicon membrane has larger thickness variations than the top layer silicon membrane, which contributes to the differences in device performance for each layer.

In summary, we present vertically integrated, two-layer, low loss, crystalline silicon membranes. We developed a DRIE recipe for fabrication of self-aligned waveguiding structures on double-bonded SOI substrates. The fabricated double-layer MMI couplers show low excess loss [0.48 dB (top) and 2.9 dB (bottom)] and uniform outputs [within 1.1 dB (top) and 1.7 dB (bottom) power fluctuation] and can be used for one-to-many fanouts on different layers in 3D silicon PICs. This approach is a potential solution to the limited silicon real estate problem via vertical integration of integrated photonic devices, such as optical phased arrays (OPAs)[24] and intra- and inter-chip guided wave optical interconnects,[25,26] which require accurate alignment between vertically integrated photonic devices.

This research is supported by the Air Force Office of Scientific Research (AFOSR) Multi-disciplinary University Research Initiative (MURI) program through the AFOSR (Contract No. FA 9550-08-1-0394).

[1] A. Shacham, B. G. Lee, A. Biberman, K. Bergman, and L. P. Carloni, in *15th Annual IEEE Symposium on High-Performance Interconnects, HOTI 2007*, 22–24 August 2007, pp. 29–38.
[2] A. Joshi, C. Batten, Y. Kwon, S. Beamer, I Shamim, K. Asanovic, and V. Stojanovic, in *NOCS "09 Proceedings of the 2009 3rd ACM/IEEE International Symposium on Networks-On-Chip*, 10–13 May 2009, pp. 124–133.
[3] D. Guckenberger, S. Abdalla, C. Bradbury, J. Clymore, P. De Dobbelaere, D. Foltz, S. Gloeckner, M. Harrison, S. Jackson, D. Kucharski, Y. Liang, C. Lo, M. Mack, G. Masini, A. Mekis, A. Narasimha, M. Peterson, T. Pinguet, J. Redman, S. Sahni, B. Welch, K. Yokoyama, and Y. Shuhuan, in *2010 36th European Conference and Exhibition on Optical Communication (ECOC)*, 19–23 September 2010, pp. 1–6.
[4] B. Analui, D. Guckenberger, D. Kucharski, and A. Narasimha, J. Solid State Circuits **41**(12), 2945–2955 (2006).
[5] A. Narasimha, B. Analui, E. Balmater, A. Clark, T. Gal, D. Guckenberger, S. Gutierrez, M. Harrison, R. Koumans, D. Kucharski, Y. Liang, A. Mekis, S. Mirsaidi, M. Peterson, T. Pham, T. Pinguet, V. Sadagopan, T. J. Sleboda, D. Song, Y. Wang, B. Welch, J. Witzens, S. Abdalla, S. Gloeckner, and P. De Dobbelaere, in *Optical Fiber Communication Conference and Exposition and The National Fiber Optic Engineers Conference, OSA* 24–28 February 2008, paper OMK7.
[6] M. Hochberg and T. Baehr-Jones, Nat. Photonics **4**, 492–494 (2010).
[7] M. K. Smit, in *21st Annual Meeting of the IEEE Lasers and Electro-Optics Society, LEOS 2008*, 9–13 November 2008, pp. 51–52.
[8] M. K. Smit, in *Photonics in Switching, OSA*, 26–28 July 2010, paper PTuA1.
[9] J. A. Kash, in *Photonics in Switching*, 19–22 August 2007, pp. 55–56.
[10] K. Preston, B. Schmidt, and M. Lipson, Opt. Express **15**, 17283–17290 (2007).
[11] J. S. Orcutt, A. Khilo, M. A. Popovic, C. W. Holzwarth, B. Moss, H. Li, M. S. Dahlem, T. D. Bonifield, F. X. Kaertner, E. P. Ippen, J. L. Hoyt, R. J. Ram, and V. Stojanovic, in *Conference on Lasers and Electro-Optics, 2008 and 2008 Conference on Quantum Electronics and Laser Science, CLEO/QELS 2008*, 4–9 May 2008, pp. 1–2.
[12] S. Zhu, Q. Fang, M. B. Yu, G. Q. Lo, and D. L. Kwong, Opt. Express **17**, 20891–20899 (2009).
[13] L. Liao, D. R. Lim, A. M. Agarwal, X. Duan, K. K. Lee, and L. C. Kimerling, J. Electron. Mater. **29**, 1380–1386 (2000).
[14] S. Selvaraja, M. Schaekers, W. Bogaerts, D. V. Thourhout, and R. Baets, in *Proceedings of 11th IEEE/LEOS Benelux Annual Workshop, IEEE/LEOS*, 25 May 2007, pp. 19–20.
[15] Q. Fang, J. F. Song, S. H. Tao, M. B. Yu, G. Q. Lo, and D. L. Kwong, Opt. Express **16**, 6425–6432 (2008).
[16] T. Tsuchizawa, K. Yamada, H. Fukuda, T. Watanabe, S. Uchyama, and S. Itabashi, Jpn. J. Appl. Phys. **45**, 6658–6662 (2006).
[17] M. Gnan, S. Thoms, D. S. Macintyre, R. M. De La Rue, and M. Sorel, Electron. Lett. **44**, 115–116 (2008).
[18] K. Preston and M. Lipson, in *Conference on Laser and Electro-Optics, 2007, CLEO 2007*, 6–11 May 2007, pp. 1–2.
[19] A. Hosseini, H. Subbaraman, D. N. Kwong, Y. Zhang, and R. T. Chen, Opt. Lett. **35**, 2864–2866 (2010).
[20] A. Hosseini, D. N. Kwong, C.-Y. Lin, B. S. Lee, and R. T. Chen, IEEE J. Sel. Top. Quantum Electron. **16**(1), 61–69 (2010).
[21] A. Brown, G. O'Neill, and S. Blackstone, Proc. SPIE **4174**, 406–415 (2000).
[22] F. Laermer and A. Urban, Microelectron. Eng. **67–68**, 349–355 (2003).
[23] I. Saraf, M. Goeckner, B. Goodlin, K. Kirmse, and L. Overzet, Appl. Phys. Lett. **98**, 161502 (2011).
[24] D. Kwong, A. Hosseini, Y. Zhang, and R. T. Chen, Appl. Phys. Lett. **99**, 051104 (2011).
[25] R. T. Chen and C. Choi, *Synthesis Lectures on Solid State Materials and Devices* (Morgan & Claypool, Austin, 2007).
[26] D. A. B. Miller, IEEE J. Sel. Top. Quantum Electron. **6**(6), 1312–1317 (2000).

Downloaded 30 Apr 2012 to 129.116.140.200. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions