# A Platform for Three-dimensional On-chip Photonics: Multi-bonded Silicon-On-Insulator wafers

**Amir Hosseini, Babak Fallahazad, David N. Kwong, Yang Zhang, Emanuel Tutuc, and Ray T. Chen**

*Microelectronics Research Center, Electrical and Computer Engineering Department, University of Texas at Austin, Austin, TX, 78758, USA*

**Corresponding authors: ahoss@mail.utexas.edu, raychen@uts.cc.utexas.edu, Fax: +1-512-471-8575*

**Abstract:** We propose a novel platform for three dimensional photonics. A double layer 1x12 multimode interference coupler is fabricated on a double-bounded Silicon-on-insulator wafer. Optical characterizations confirm low insertion loss and uniform outputs.

**OCIS codes:** (130.3120) Integrated optics devices; (130.2790) Guided waves

## 1. Introduction

Large on- and off-chip bandwidths required for high performance multi-core structures (~10TB/s by 2015) that correspond to interconnect energy budgets of ~100 fJ/bit will render optical components essential parts of future high performance integrated systems [1]. CMOS compatible silicon photonics, which allows for integration of optical components on the same SOI wafer with COMS transistors, is considered as the solution for such high demand for such low energy and high bandwidth communications [2]. Since the first from Luxtera's silicon photonic chip in 2002, the number of on-chip photonic components has doubled each year [3]. There is also a Moore's law like trend observed in the InP-based photonic IC development since 1988 [4]. However, due to the large sizes of the on-chip photonic components, single layer photonic component counts cannot exceed beyond about 1000 and 10000 in InP and silicon photonic ICs, respectively [5]. Vertical integration of multiple layers of active and passive components can resolve the problem of limited real estate on a single layer [6]. So far, an extra polysilicon layer on top of the crystalline silicon layer has been used for CMOS microelectronics and photonics integration [7]. This scheme may also be used for 3D photonics integration. However, the optical losses in polysilicon waveguide are dominated by scattering and absorption at the grain boundaries [7], which increases significantly when the waveguide width shrinks to 200nm [8]. Propagation losses from 7dB to 13dB in polycrystalline silicon waveguides were reported [8] [9], which are by average 9dB more than those in crystalline silicon nano-wire waveguides. Additionally, if the temperature process is limited to about 600°C, which is compatible with standard CMOS processes, the quality factor of the ring resonators fabricated on polysilicon layers drops by a factor of 5 [7].

In this paper we demonstrate the possibility of 3D photonic integration of self aligned-structures using multi-bonded SOI wafers. We fabricate 2-layers of 1x12 low loss and uniform multimode-interference (MMI) couplers. Using the presented scheme, multi-levels of bulky photonic components such as large MMI couplers and AWGs can be vertically integrated, which allows for increasing of on-chip photonic components count.

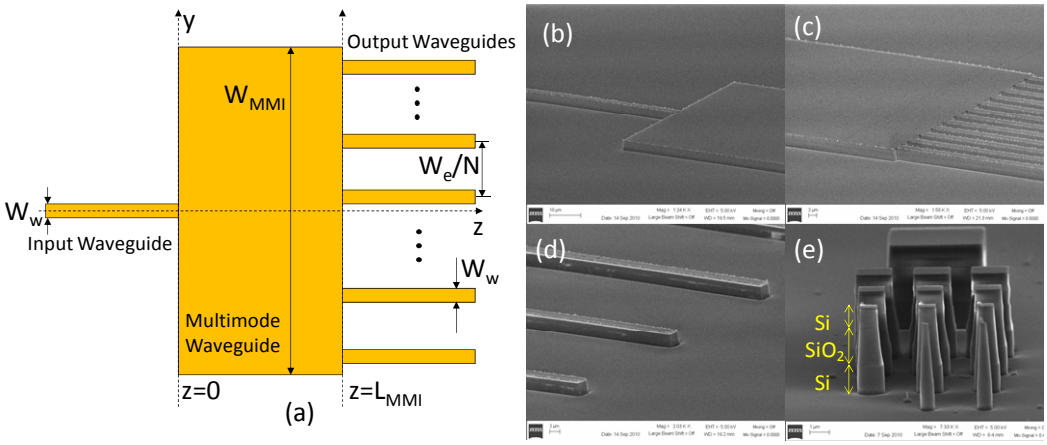


Fig. 1. (a) A schematic of 1x12 MMI coupler. $W_{MMI}$=60µm, $L_{MMI}$=560µm, $W_w$=2.4µm. . SEM images of (b) MMIs' input, (c) MMIs' output, (d) output waveguides termination before the silicon etch on the top layer only, (e) a cross-section view of test structures.

© Optical Society of America

## 2. Design and fabrication process

We form two self-aligned 1x12 MMI couplers on the silicon layers. MMI couplers can be used for efficient on-chip beam splitting. A schematic of a 1xN MMI coupler is shown in Figure 1(a). We choose MMI width, $W_{MMI}$=60µm. The MMI Length is given as $L_{MMI} = (n_{eff}W_{MMI}^2)/(\lambda_0 N)$, where, $n_{eff}$ is the effective index of the multimode waveguide, N=12 is the number of outputs and $\lambda_0$=1.55µm is the free space wavelength. A fanout design is used to increase the separation of output channels to 30µm. The double bounded SOI wafers are provided by Ultrasil, and are fabricated using fusion bonding and etch-back. The thicknesses of the silicon and silicon dioxide layers are 1.3 µm and 2.0µm respectively. An etching mask is defined through the e-beam lithography, deposition of 100nm-thick chromium, and a lift-off process. The sample is then transferred into Plasma-Therm VERSALINE ICO chamber for deep Reactive Ion Etching (RIE) of the silicon films and also etching of the top silicon oxide. The chuck temperature was maintained at 10°C during the process and both silicon and silicon oxide films are etched through a two step polymer deposition/etching cycle. The etch rate of silicon and silicon oxide are ~150nm/cycle and ~2.2nm/cycle, respectively. SEM pictures of the fabricated double layer MMIs are shown in Figure 2(b-d). The cross-section SEM image of test structures in Figure 2(e) shows negligible undercut etching for the MMI performance.

## 3. Optical characterization

A six-axis automated aligner system with a 50nm precision in movement was used to couple TE polarized light at 1550nm from a polarization maintaining lensed fiber (PMF) with a 2.5µm output mode diameter into the waveguide inputs. An IR CCD camera connected to a variable objective lens captured the top-down near field images of the cleaved output waveguides' facets. In order to separate the outputs in the bottom layer from those in the top layer, we etch the output waveguides of the top layer to terminate them before where the bottom layer waveguides end as shown in Fig. 2(a). Figure 2(b) shows results of simultaneous excitation of top and bottom layers. Efforts are underway to characterize (insertion loss and uniformity) by fiber scanning. As shown in Figure 3, the 12 uniform outputs from the top and bottom MMI couplers are separated from each other along the output waveguides.
In summary, we presented the first vertical integration of bulky photonic devices on multi-levels of low loss crystalline silicon nanomembranes. This scheme is a potential solution to the limited silicon real estate for high photonics integration.

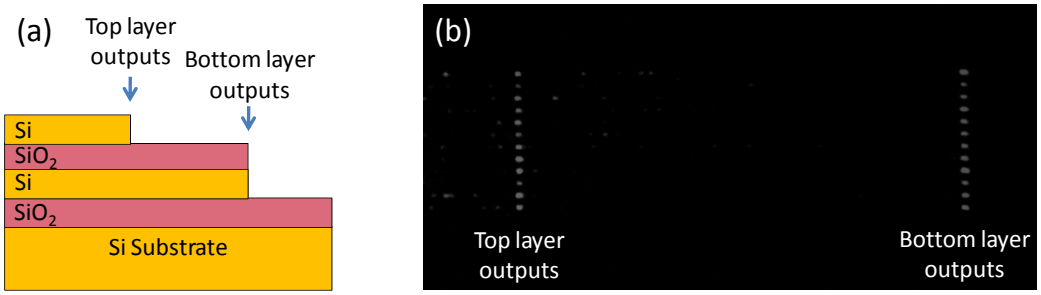


Fig. 2. (a) Across-section schematic showing termination of the output waveguides on the top and bottom layers. (b) An IR top down image of the 2 1x12 MMI couplers with simultaneous excitation. The separation between the outputs at each layer is 30µm.

## 4. References

[1] A. Shacham, B. G. Lee, A. Biberman, K. Bergman, L. P. Carloni, "Photonic NoC for DMA Communications in Chip Multiprocessors," 15th Annual IEEE Symposium on High-Performance Interconnects (HOTI 2007), 29-38 (2007).

[2] B. Analui, D. Guckenberger, D. Kucharski, and A. Narasimha, "A Fully Integrated 20-Gb/s Optoelectronic Transceiver Implemented in a Standard 0.13-um CMOS SOI Technology", Journal of Solid-State Circuits (JSSC) **41**(12), 2945-2955 (2006).

[3] M. Hochberg and T. Baehr-Jones, "Towards fabless silicon photonics," Nature Photonics **4**, 492 - 494 (2010).

[4] M. K. Smit, "Past and future of InP-based Photonic Integration," 21st Annual Meeting of the IEEE Lasers and Electro-Optics Society (LEOS), 51-52 (2008).

[5] M. K. Smit, "Switching to Low-Cost Integration Technology for Switching," OSA Photonics in Switching, PTuA1 (2010).

[6] J. A. Kash, "IntraChip Optical Networks for a Future Supercomputer-on-a-Chip,"OSA Photonics in Switching, 55 – 56 (2010).

[7] K. Preston, B. Schmidt, and M. Lipson, "Polysilicon photonic resonators for large-scale 3D integration of optical networks," Opt. Express **15**, 17283-17290 (2007).

[8] S. Zhu, Q. Fang, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Propagation losses in undoped and n-doped polycrystalline silicon wire waveguides," Opt. Express **17**, 20891-20899 (2009).

[9] Q. Fang, J. F. Song, S. H. Tao, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Low loss (~6.45dB/cm) sub-micron polycrystalline silicon waveguide integrated with efficient SiON waveguide coupler," Opt. Express **16**, 6425-6432 (2008).